WHAT IS CLAIMED IS:

1. A control signal unit, comprising:

a substrate;

a signal line formed on said substrate;

an insulating layer covering said signal line;

a contact hole exposing the signal line with a predetermined width, said contact hole having a lateral side bordering on said signal line, the lateral side of the contact hole being longer than the width of the contact hole; and

a subsidiary signal pad connected to said signal line through said contact hole.

2. The control signal unit of claim 1, wherein the lateral side of the contact hole has an inclined portion proceeding in the direction of the width.

3. The control signal unit of claim 1, wherein the contact hole has a protruded portion proceeding in the longitudinal direction of said signal line.

4. The control signal unit of claim 3, wherein at least one side of the protruded portion is overlapped with said signal line.

5. The control signal unit of claim 1, wherein said signal line has a double-layered structure with an under-layer and an over-layer, and the contact hole is formed at said insulating layer, and the over-layer of said signal line.

6. The control signal unit of claim 5, wherein the over-layer of said signal line is formed with an aluminum-based metallic material.

7. A control signal unit, comprising:

a substrate;

a plurality of signal lines formed on said substrate;

an insulating layer covering the signal lines;

contact holes exposing the respective signal lines, each of which has a predetermined width, each contact hole having a lateral side bordering on the signal line, the lateral side of each contact hole being longer than the width of the contact hole; and

subsidiary signal pads connected to the respective signal lines through the respective contact holes.

8. The control signal unit of claim 7, further comprising a signal transmission film with signal leads, the signal leads being connected to the signal lines in one to one correspondence.

9. The control signal unit of claim 8, wherein the signal leads of the signal transmission film comprises a first signal lead carrying high voltage signals and a second signal lead carrying low voltage signals, and a dummy lead is formed between the first signal lead and the second signal lead.

10. The control signal unit of claim 9, wherein the same voltage is applied to the dummy lead and the first signal lead.

11. The control signal unit of claim 10, wherein the dummy lead is several to several tens micrometers thick.

12. The control signal unit of claim 10, wherein a dummy line

corresponding to the dummy lead is formed at the substrate.

13. The control signal unit of claim 12, wherein the dummy line is formed with a conductive material that is less oxidative than the signal line.

14. A liquid crystal display, comprising:

a substrate;

a gate line assembly and a plurality of signal lines formed on the substrate, the gate line assembly comprising gate electrodes and gate lines;

a gate insulating layer covering the gate line assembly and the signal lines;

thin film transistor semiconductor patterns formed on the gate insulating layer;

a data line assembly comprising data lines crossing over the gate lines while being insulated from the gate lines, source electrodes extended from the data lines while contacting the semiconductor patterns, and drain electrodes contacting the semiconductor patterns in correspondence with the source electrodes;

a protective layer covering the data line assembly and the semiconductor patterns;

first contact holes exposing the drain electrodes;

second contact holes exposing the respective signal lines with a predetermined width, the contact hole having a lateral side bordering on the signal line, the lateral side of the contact hole having a length greater than the width of the contact hole; and

pixel electrodes and subsidiary signal pads standing in the same plane, the pixel electrodes being connected to the drain electrodes, the subsidiary signal pads being connected to the signal lines.

15. The liquid crystal display of claim 14, wherein the gate line assembly and the signal lines have a double-layered structure with an aluminum-based layer.

16. The liquid crystal display of claim 15, wherein the second contact holes are formed at the gate insulating layer, the protective layer, and the aluminum-based layer of the signal lines.

17. The liquid crystal display of claim 14, further comprising a signal transmission film with signal leads, the signal leads connected to the signal lines in one to one correspondence.

18. The liquid crystal display of claim 14, wherein the signal leads of the signal transmission film comprise a first signal lead carrying high voltage signals and a second signal lead carrying low voltage signals, and a dummy lead is formed between the first signal lead and the second signal lead.

19. The liquid crystal display of claim 18, wherein the same voltage is applied to the dummy lead and the first signal lead.

20. The liquid crystal display of claim 18, wherein the dummy lead is several to several tens micrometers thick.

21. The liquid crystal display of claim 18, wherein a dummy line corresponding to the dummy lead is formed at the substrate.

22. The liquid crystal display of claim 21, wherein the dummy line is formed with a conductive material that is less oxidative than the signal line.

23. The liquid crystal display of claim 14, further comprising:

a gate pad connected to each gate line as a component of the gate line assembly;

a data pad connected to each data line as a component of the data line assembly;

a third contact hole exposing said gate pad with a predetermined width;

a fourth contact hole exposing said data pad with a predetermined width;

a subsidiary gate pad covering said gate pad at the third contact hole; and

a subsidiary data pad covering said data pad at the fourth contact hole.

24. The liquid crystal display of claim 23, wherein each of the third contact hole and the fourth contact hole has a lateral side bordering on the pad, the lateral side of the contact hole being longer than the width of the contact hole.

25. The liquid crystal display of claim 14, further comprising:

common voltage pads formed at the substrate, the common voltage pads being covered by one insulating layer among the gate insulating layer and the protective layer;

contact holes formed at the insulating layer with a predetermined width while exposing the common voltage pads, each contact hole having a lateral side bordering on the pad, the lateral side of the contact hole being longer than the width of the contact hole; and

subsidiary common voltage pads connected to the common voltage pads through the contact holes.

26. The liquid crystal display of claim 25, further comprising a color filter

substrate with a common electrode, the common electrode being connected to the subsidiary common voltage pads.

27. A method for fabricating a liquid crystal display, comprising the steps of:

forming a gate line assembly and signal lines on a substrate, the gate line assembly comprising gate electrodes and gate lines;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the signal lines;

forming semiconductor patterns on the gate insulating layer;

forming a data line assembly with data lines crossing over the gate lines, source electrodes contacting the one-sided semiconductor patterns, and drain electrodes contacting the other-sided semiconductor patterns in correspondence with the source electrodes;

forming a protective layer such that the protective layer covers the data line assembly and the semiconductor patterns;

forming first contacting holes and second contact holes with a predetermined width such that the first contact holes expose the drain electrodes, and the second contact holes expose the signal lines; and

forming pixel electrodes and subsidiary signal pads such that the pixel electrodes are connected to the drain electrodes through the first contact holes, and the subsidiary signal pads are connected to the signal lines through the second contact holes.

28. The method of claim 27, wherein each second contact hole has a lateral side bordering on the signal line, the lateral side of the contact hole being longer

than the width of the contact hole.

29. The method of claim 28, wherein the signal lines have a double-lined structure with an aluminum-based layer, and the second contact holes are formed through dry-etching the gate insulating layer and the protective layer covering the signal lines while exposing the aluminum-based layer, and wet-etching the exposed portions of the aluminum-based layer using an aluminum etching solution.

30. The method of claim 27, wherein the gate line assembly further comprises gate pads connected to the gate lines, and the data line assembly further comprises data pads connected to the data lines, the method further comprising the steps of:

forming third contact holes and fourth contact holes with a predetermined width at the step of forming the first contact holes and the second contact holes such that the third contact holes expose the gate pads, and the fourth contact holes expose the data pads; and

forming subsidiary gate pads and subsidiary data pads at the step of forming the drain electrodes and the subsidiary signal pads such that the subsidiary gate pads cover the gate pads, and the subsidiary data pads cover the data pads.

31. The method of claim 30, wherein each of the third contact holes and the fourth contact holes has a lateral side bordering on the pad, the lateral side of the contact hole being longer than the width of the contact hole.

32. The method of claim 27, wherein the semiconductor patterns and the data line assembly are formed together using photoresist patterns of different thickness.

33. The method of claim 32, wherein the photoresist patterns comprise a first photoresist pattern placed over the data line assembly with a first thickness, and a second photoresist pattern placed over the channel portion between the source and the drain electrodes with a second thickness, the second thickness being smaller than the first thickness.

34. The method of claim 32, wherein the semiconductor patterns and the data line assembly is formed through the steps of:

depositing a semiconductor layer and a conductive layer onto the gate insulating layer, and forming the photoresist patterns on the conductive layer;

etching the conductive layer using the photoresist patterns as a mask such that the semiconductor layer is partially exposed to the outside;

removing the exposed portions of the semiconductor layer and the second photoresist pattern to complete the semiconductor patterns while exposing the portions of the conductive layer placed between the source and the drain electrodes;

removing the exposed portions of the conductive layer to complete the data line assembly; and

removing the first photoresist pattern.

35. The method of claim 34, wherein the photoresist patterns are made using a mask with a first region, a second region and a third region, the first region of the mask having a light transmission higher than the second region but lower than the third region.